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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,492	03/01/2004	Lingyi A. Zheng	MIO 0082 N2/40509.292	9512

7590 07/22/2005

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/790,492	ZHENG ET AL.
	Examiner	Art Unit
	Toniae M. Thomas	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/790,492, which is a continuation of Application Serial No. 10/228,911 filed on 27 August 2002, now abandoned, which is a divisional of Application Serial No. 09/994,547 filed on 27 November 2001, now US Patent No. 6,551,893.

2. Currently, claims 1-11 are pending.

Information Disclosure Statement

3. The information disclosure statement (IDS) filed 07 June 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed (see MPEP § 609, subsection III A (2)). Accordingly, the non-patent literature documents cited in the IDS have not been considered.

4. In response to this Office action, Applicants are required to submit a copy of the non-patent literature documents, along with a copy of the PTO-1449 form filed on 07 June 2004, for examiner's consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

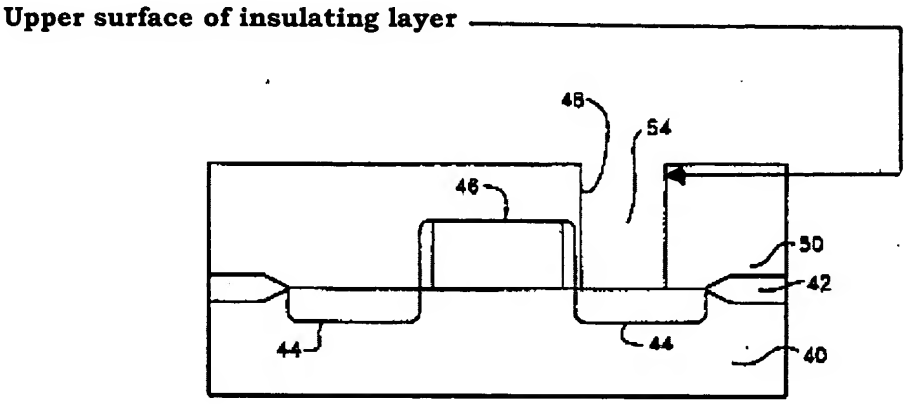
5. Claims 1 and 3-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al. (US 5,624,865) in view of Lee et al. (US 2002/0068466 A1).[1]

The Schuegraf et al. patent (Schuegraf) discloses a process for forming a memory cell (figs. 4-9 and accompanying text). The method comprises: forming a semiconductor structure defining a transistor 46 and a pair of transistor node locations 44 in a semiconductor substrate 40 (fig. 4 and col. 5, lines 5-8); forming an insulating layer 50 over the semiconductor substrate, wherein in one preferred embodiment the insulating layer is BPSG (fig. 5 and col. 5, lines 15-25); forming a container 54 in the insulating layer over one of the transistor node locations (fig. 5 and col. 5, lines 15-25); forming a polysilicon lower electrode layer 58 along an inner surface of the container, wherein in one preferred embodiment the polysilicon is HSG polysilicon (fig. 6; col. 5, lines 27-34; and col. 5, lines 40-48); forming a dielectric layer 64 characterized by a given degree of uniformity over the polysilicon lower electrode layer and an upper surface of the insulating layer, wherein in a preferred embodiment the dielectric layer is a silicon nitride layer and has a thickness that is sufficient to prevent oxidation punch-through from a reoxidized layer 68 formed over the dielectric layer to the polysilicon lower electrode layer (fig. 8; col. 6, lines 1-4; col. 10, lines 9-11; and col. 6, lines 19-21); and forming an upper electrode

[1] Applicant submitted both the Schuegraf et al. reference and the Lee et al. reference as prior art (see information disclosure statement filed on 07 June 2005).

layer 72 over the reoxidized layer 68 (fig. 9 and col. 6, lines 21-28). The silicon nitride layer may have a thickness less than about 50 angstroms (col. 6, lines 19-21).

The lower electrode layer 58 is formed so as to extend along an upper surface of the insulating layer 50 and from the inner surface 48 in the direction of the upper surface of the insulating layer along an extension of the container 54 (see fig. 7).



The dielectric layer 64 is formed on the lower electrode layer (see fig. 8).

Schuegraf lacks anticipation of forming the silicon nitride dielectric layer 64 through an atomic layer deposition (ALD) process, where a silicon-containing precursor is chemisorbed over a surface of the lower electrode layer and a nitrogen-containing precursor is reacted with the chemisorbed silicon-containing precursor to form the silicon nitride dielectric layer. The Lee et al. pre-grant published application (Lee), on the other hand, teaches forming a silicon nitride dielectric layer through an ALD process (see figs. 2A-2F and accompanying text). Lee discloses an ALD method for depositing a silicon

nitride layer, where first a silicon-containing precursor is chemisorbed over a surface of substrate (fig. 2A and par. 25, lines 9-13), and then a nitrogen-containing precursor is reacted with the chemisorbed silicon-containing precursor to form a silicon nitride dielectric layer (fig. 2E and par. 27, lines 1-6). The resulting silicon nitride is about 2 angstroms thick (par. 28, lines 1-11). However, the ALD process may be repeated until a desired thickness is achieved (par. 28, lines 4-11). Moreover, the resulting silicon nitride layer is a high quality film having good step coverage (par. 28, lines 4-8).

As compared with conventional chemical vapor deposition (CVD) methods, for example low-pressure chemical vapor deposition (LPCVD), thin films deposited using ALD methods have excellent step coverage and uniformity (Lee - par. 3, line 8 - par. 5, line 7). Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Schuegraf by forming the silicon nitride layer using an ALD process, as taught by Lee, since thin films deposited using ALD have excellent step coverage and uniformity.

6. *Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf in view of Lee as applied to claim 1 above, and further in view of Thakur (US 5,407,534).*

Schuegraf lacks anticipation of forming the lower electrode layer such that it extends beyond the inner surface of the container. However, Thakur teaches forming a lower electrode layer such that it extends beyond the inner

surface of a container (see figs. 2-4 and accompanying text). Thakur discloses a process for forming a capacitor, wherein the method comprises: forming a semiconductor structure defining a transistor 21 and a transistor node location 24 in a semiconductor substrate 20 (fig. 2 and col. 3, lines 33-35); forming a BPSG insulating layer 22 over the semiconductor substrate 20 (fig. 2 and col. 3, lines 35-38); forming a container in the insulating layer over the transistor node location (fig. 2 and col. 3, lines 38-39); and forming an HSG polysilicon lower electrode layer 23 along an inner surface of the container (figs. 2, 3 and col. 3, lines 39-51). The lower electrode layer 23 extends beyond the inner surface of the container (figs. 2, 3 and col. 3, lines 39-42).

Both Schuegraf and Thakur disclose a process for forming a memory cell in a dynamic random access memory (DRAM) device, the memory cell comprising a storage node capacitor, wherein the storage capacitor has as its storage node capacitor cell plate an HSG polysilicon lower electrode layer connected to a transistor node. As Thakur points out, "in dynamic semiconductor memory storage devices it is essential that storage node capacitor cell plates be large enough to retain an adequate charge (or capacitance) in spite of parasitic capacitances and noise that may be present during circuit operation" (Thakur - col. 1, lines 27-32). The surface area of the storage node capacitor cell plate is directly proportional to capacitance, that is, increasing the surface area of the cell plate increases capacitance ($C=\varepsilon\varepsilon_o A/d$). Thus, it follows that forming the lower electrode layer to extend beyond the

surface of the container increases the surface area of the cell plate and, thereby increases capacitance. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Schuegraf and Lee by forming the lower electrode layer so that it extends beyond the surface of the container, as taught by Thakur, since doing so increases the surface area of the storage node capacitor cell plate and thereby increases capacitance.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application (see 37 CFR 1.130(b)).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. *Claims 1-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 6,551,893 B1 (Zheng et al.) in view of US Patent No. 5,407,534 (Thakur).* The claimed invention in the Zheng et al. patent (Zheng) differs from the claimed invention in the current application in that the patented claims do

not recite the limitation "wherein said lower electrode layer is formed so as to extend beyond said inner surface of said container." However, as explained above, Thakur teaches forming a lower electrode layer, such that extends beyond the inner surface of a container.

It would have been obvious, at the time the invention was made, to modify the Zheng patent by reciting the claim limitation "wherein said lower electrode layer is formed so as to extend beyond said inner surface of said container," as taught by Thakur, since this limitation offers the improvement of increased capacitance of the storage node capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
22 June 2005

Mary Wilczewski
Primary Examiner